AC-DC Converter with Internal HV Start-up Circuit

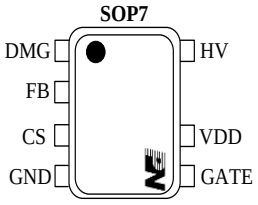
General Description

The PN8273 consists of an integrated current mode Pulse Width Modulator (PWM) controller and high voltage start circuit, specifically designed for a high performance off-line converter with minimal external components.

PWM, PFM, Burst-mode operation and low consumption device help to meet the standby energy saving standards and achieve higher efficiency. Excellent EMI performance is achieved by frequency modulation and soft driver technique.

The PN8273 offers completed and excellent protections including Brown-in/out, AC Line OVP, external over temperature protection, Cycle-by-Cycle current limiting, over load protection.

Package/Order Information



Order codes	Package
PN8273SS-P1	SOP7
PN8273SS-B1	SOP7

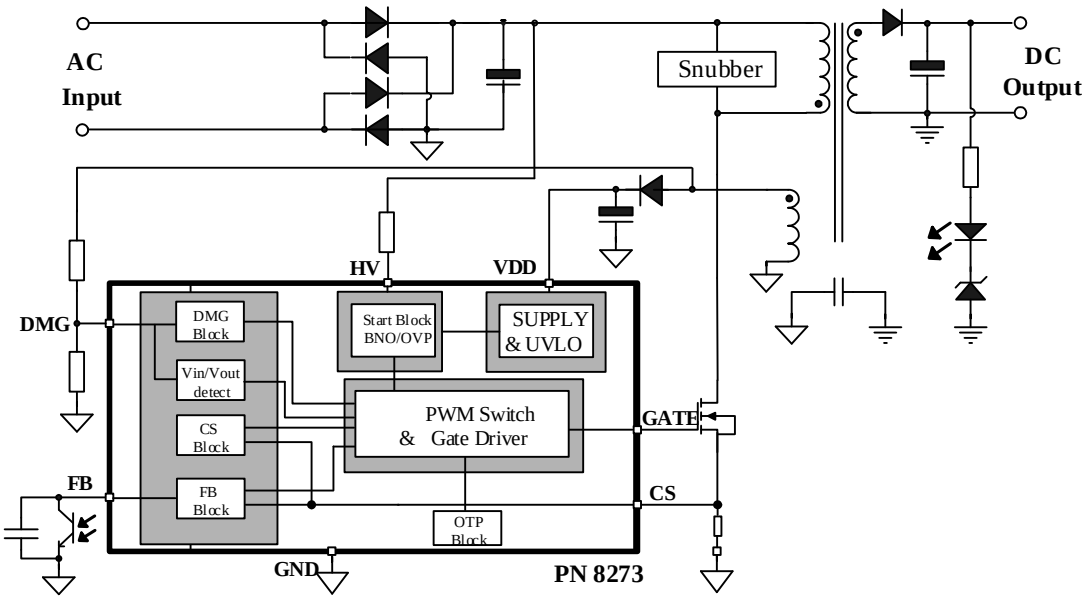
Features

- Internal HV Start-up Circuit
- Multi-mode Operation to Achieve Higher Efficiency
- No-load Consumption Power < 50mW @230VAC
- Proprietary Frequency Jitter for EMI
- VDD Operating Voltage Range 8~40V
- Adjustable AC Line Input Compensation
- Excellent Protection Coverage
  - ✧ Over Temperature Protection (OTP)
  - ✧ Brown-In/Out Protection
  - ✧ Output Over Voltage Protection
  - ✧ Cycle-by-cycle Over Current Protection (OCP)
  - ✧ Output Open/short Protection
  - ✧ Patented DMG Resistor Short Protection
  - ✧ Secondary Rectifier Short Protection
  - ✧ Over Load Protection（OLP）

Applications

- Stand-by Power
- Open-frame SMPS
- Adaptor

Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
DMG	1	Demagnetization pin. Input and output voltage detection by the voltage divider resistors.
FB	2	Voltage feedback.
CS	3	Current sense input
GND	4	Ground
GATE	5	Totem-pole gate drive output for the power MOSFET.
VDD	6	Positive supply voltage input
HV	7	High voltage start pin. High voltage startup.

Note：HV cannot be connected to the positive terminal of high voltage electrolytic after Rectifier Bridge.

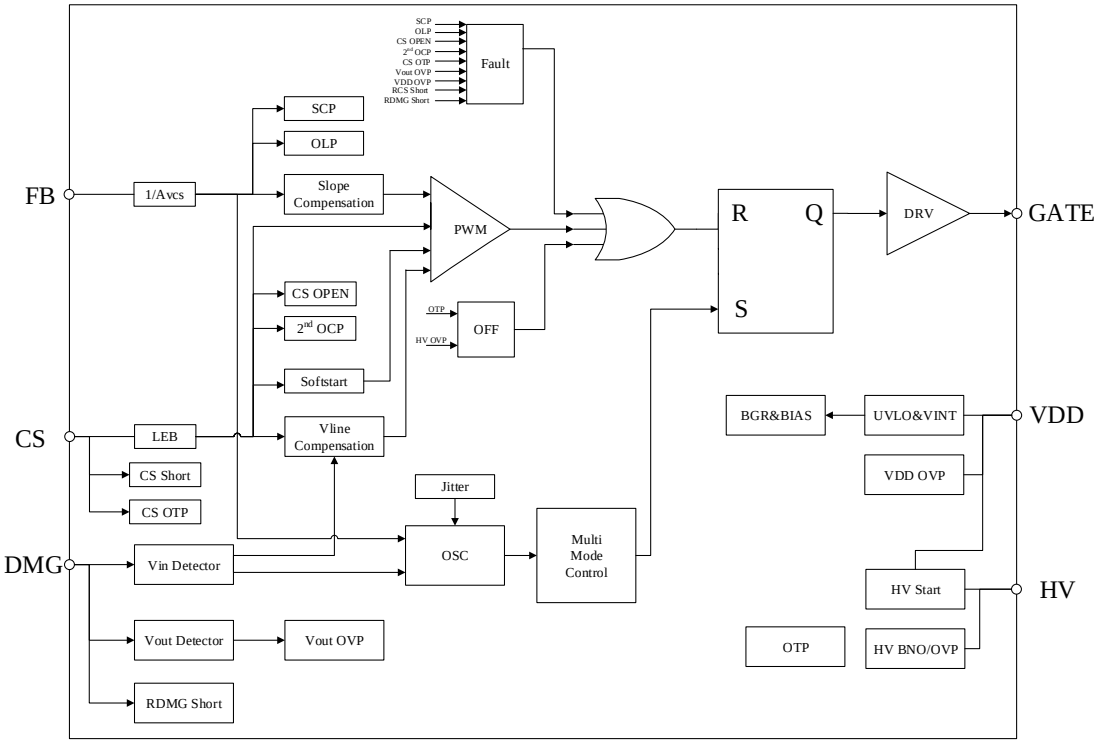
Typical Power

Part Number	Input Voltage	Adapter(1)
PN8273	90-265 V_{AC}	120W

Note:

1. Typical output power is tested in an adapter at 40℃ ambient temperature, with enough cooling conditions.

Block Diagram



Absolute Maximum Ratings

Supply voltage Pin VDD ……....-0.3~43V
Pin FB, CS……..….-0.3~6.5V
Pin DMG (I_{DMG}≤10mA)……-1~6.5V
Pin GATE ……..……..-0.3~15V
Pin HV ……..……-0.3~800V
Operating Junction Temperature ……..……-40~150°C
Storage Temperature Range…….……..……-55~150 °C
Lead Temperature (Soldering, 10Secs)……....260 °C
Package Thermal Resistance θ_{JC} (SOP7)……40°C /W
HBM ESD Protection (1) ……..... ±4kV
MM ESD Protection (2)……300V

Note:

1. Test standard: JEDEC JS-001-2017.
2. Test standard: JESD22-A115C-2010.

Electrical Characteristics

(T_A=25°C, VDD=15V, unless otherwise specified)

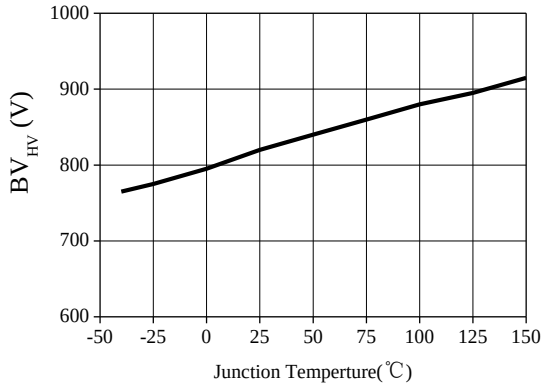
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HV Section						
Break-down voltage	BV_{HV}	I_{HV} = 250uA	800	830		V
Start up charging current	I_HV	VDD=VDD_{off} - 1	1	1.5	2	mA
Off-state current	I_{OFF}		5	18	30	μA
HV Section - AC Line OVP						
HV OVP voltage	V_OVP	DC Level	437	450	473	V
HV OVP hysteresis voltage	V_OVP_hys	DC Level		40		V
HV Section - Brown in/out						
Brown In voltage	V_{BNI}	Rhv=10kΩ	98	104	116	V
Brown In enabling duration	Td_BNI			150		us
Brown Out voltage	V_{BNO}		76	85	96	V
Brown Out enabling duration	Td_BNO		90	135	200	ms
VDD Supply Voltage Section						
VDD start up threshold	VDD_{on}		17	18	19	V
VDD under voltage shutdown threshold	VDD_{off}		7.0	8.0	9.0	V
VDD OVP Voltage	VDD_{ovp}		38.0	40.5	43.0	V
VDD threshold for continuous work under BM	Vhold-up		7.5	9	10.5	V
VDD Supply Current Section						
Operating supply current, switching	I_{VDD0}		1	1.5	3.0	mA
Operating supply current, under burst mode	I_{VDD1}		0.1	0.65	1.5	mA
Operating supply current, with protection tripping	I_{VDD_Fault}	After OVP	0.1	0.8	1.5	mA
Oscillator Section						
Switching frequency	F_{osc}		60	65	70	kHz
Burst mode frequency	Fosc_BM		20	24	28	kHz
Jitter frequency	F_jitter		24	30	36	Hz
Frequency modulation range	$\triangle F_{osc}$			±6		%

Electrical Characteristics (Continued)

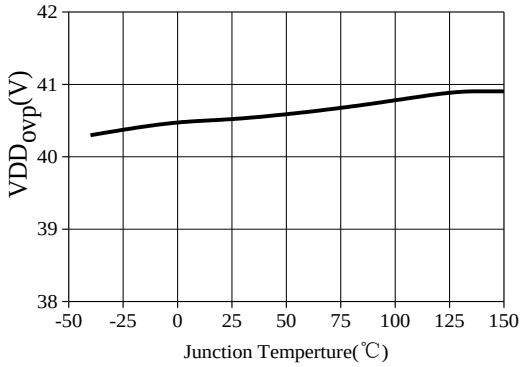
(T_A= 25°C, VDD=15V, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FB Section						
FB loop voltage	V_{FB}		4.8	5.2	5.4	V
FB short current	I_{FB_SHORT}		0.14	0.2	0.26	mA
Maximum duty cycle	Dmax		70	80	90	%
Green mode entry voltage	V_{FB_PFM}		2.3	2.5	2.7	V
Burst mode entry voltage	$V_{FB\_BM\_L}$		1.05	1.15	1.25	V
Burst mode ending voltage	$V_{FB\_BM\_H}$		1.15	1.25	1.35	V
OLP threshold voltage	Vth_OLP		4.1	4.4	4.7	V
OLP De-Bounce time	Td_OLP		48	60	72	ms
Current Sense Section						
Soft-start time	Tss		6.4	8	9.6	ms
Leading edge blanking time	TLEB			320		ns
Internal current limiting threshold voltage	Vth_OCP		0.72	0.75	0.78	V
Threshold voltage of secondary rectifier short protection	V_{DSP}			1.1		V
De-Bounce time of SRCP	Td_DSP			7		Cycles
CS OTP threshold voltage	V_CSOTP		0.8	0.82	0.84	V
CS OTP De-Bounce time	Td_CSOTP			48		ms
DMG Section						
DMG OVP voltage	V_{DMG_OVP}		2.85	3	3.15	V
De-Bounce time of DMG OVP	Td_DOVP			7		Cycles
Minimum turn ON time	Ton_max		10	12	14	us
GATE Section						
Output clamp voltage level	V_clamping		11	13	15	V
Output rising time	T_r	CL=1000pF		130		ns
Output falling time	T_f	CL=1000pF		40		ns
Thermal Section						
Thermal shutdown temperature	T_{SD}		130	145		℃
Thermal shutdown hysteresis	T_{HYST}			30		℃

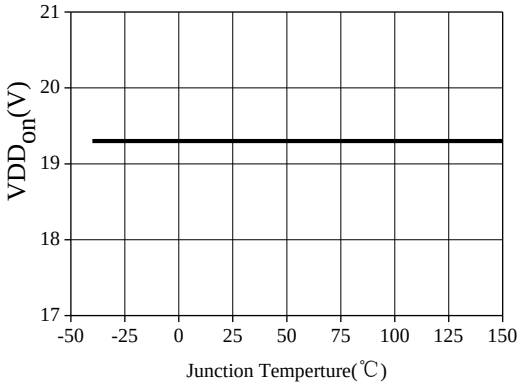
Typical Characteristics



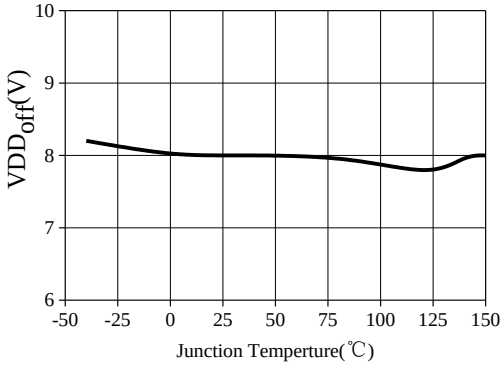
(a) BV_{HV} vs T_j



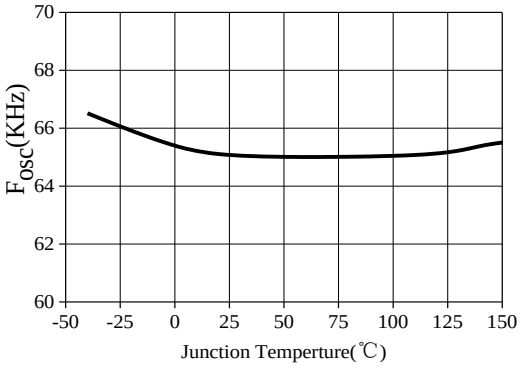
(b) VDD_{ovp} vs T_j



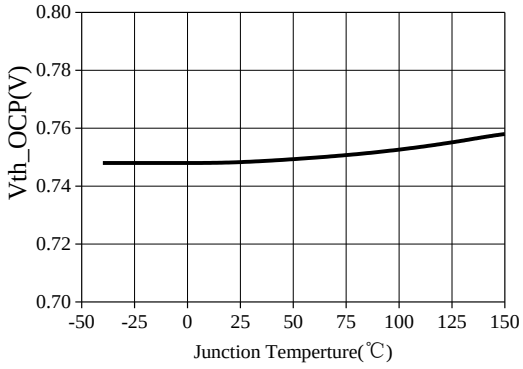
(c)VDD_{on} vs T_j



(d) VDD_{off} vs T_j



(e) F_{OSC} vs T_j



(f) Vth_OCP vs T_j

Functional Description

1. Start up

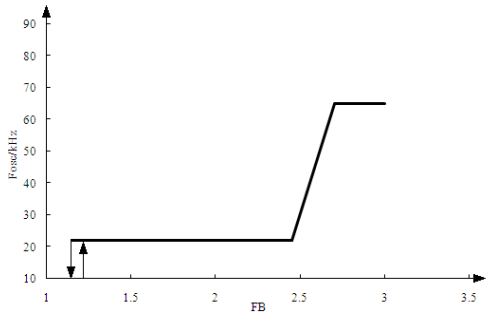
At start up, the internal high-voltage current source supplies the internal bias and charges the external VDD capacitor. When VDD reaches VDD_{on}, the device starts switching and the internal high-voltage current source stops charging the capacitor. After start up, the bias is supplied from the auxiliary transformer winding.

2. Soft-start up

In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and prevent the transformer turning into the saturation state. Typically, the duration of soft-start is 8ms.

3. Oscillator

The switching frequency of PN8273 is internally fixed. The frequency is 65kHz. PFM operation helps to meet the standby energy saving standards and achieve higher efficiency. When FB is less than V_{FB_PFM}, the PN8273 enter PFM. Lighter the load, less the switching frequency. The minimum switching frequency is closed at Fosc_BM.



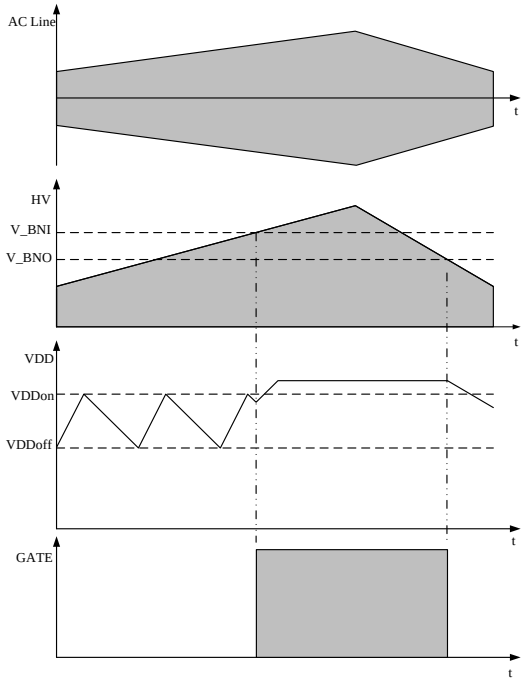
The PN8273 enters burst-mode operation in order to minimize the power dissipation in standby mode. As the load decreases, the feedback voltage decreases. When the voltage on FB pin falls below $V_{FB\_BM\_L}$ (1.15V typically), the device enters burst mode and power MOSFET stops switching. It can be switched on again once the voltage on FB pin exceeds $V_{FB\_BM\_H}$.

4. AC Line OVP (PN8273SS-P1)

PN8273 integrates input voltage detection module to realize AC Line OVP function. When the HV voltage is higher than V_OVP, the GATE output will stop switching; when AC Line Voltage decreases, PN8273 detects that the HV voltage is less than V_OVP-V_OVP_hys, and the GATE output will start switching again.

5. Brown-In/Out Protection (PN8273SS-B1)

The PN8273 features Brown-in/out function on HV pin. When HV < V_{BNI}, GATE pin will remain off even when the VCC already reaches VDD_{on}. It therefore forces the VDD hiccup between VDD_{on} and VDD_{off}. Unless the next VDD_{on} is tripped and the line voltage rises over V_{BNI}, GATE pin will start switching. A hysteresis is implemented to prevent the false-triggering.



6. Gate driver

The internal power MOSFET in the PN8273 is driven by a dedicated gate driver for power switch control. A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

7. Over Load Protection

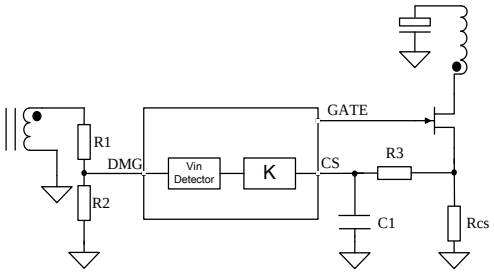
Overload is defined as the load current exceeding a pre-set level due to an accident event as a fault. If FB exceeds Vth_OLP for more than Td_OLP (de-bounce time of OLP), the protection circuit should be activated to protect the SMPS.

8. Internal Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the feedback voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

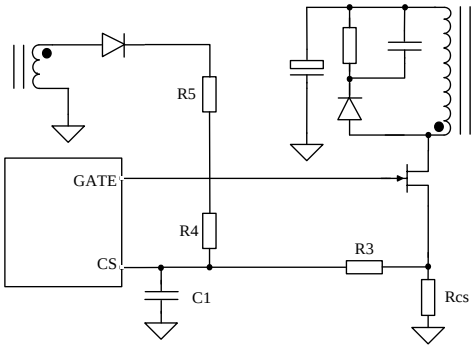
9. Line Input Compensation

The PN8273 offers Line Input Compensation; this feature improves the power limit constant output. The PN8273 detects the input voltage across DMG pin and generate the compensated current. Thus the compensated current can be calculated as $I_{LC}=K*I_{DMG}$, where K is the compensated coefficient. I_{LC} multiplied R3 equals the compensated voltage that can limit the pulse-by-pulse current.

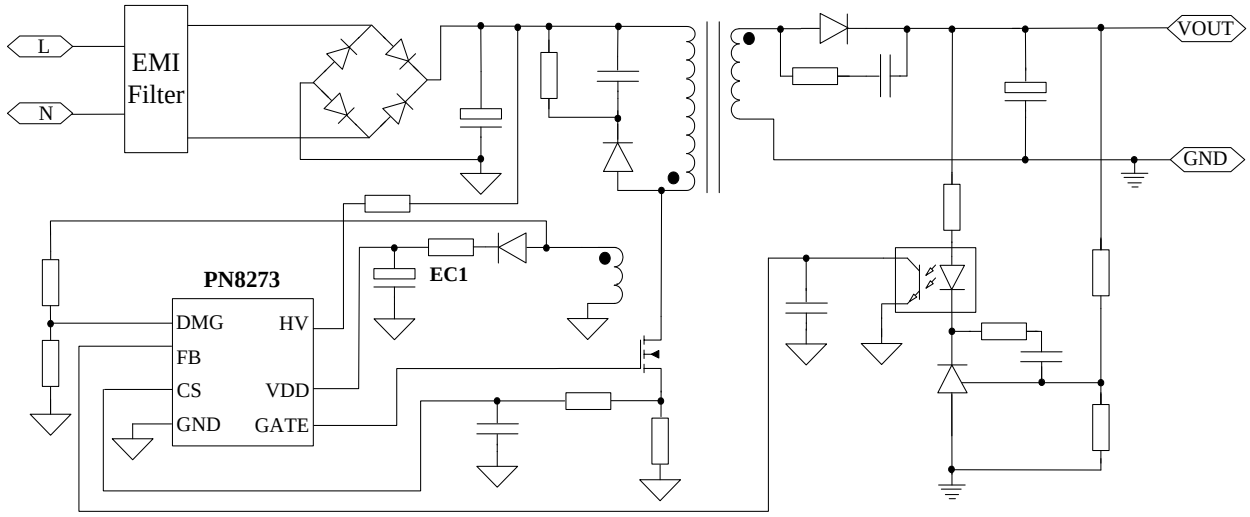


10. Over Temperature Protection

Both an internal OTP circuit and an external OTP circuit are embedded inside the PN8273 to prevent the system from hot damage. If the temperature exceeds about 145℃， OTP fault is activated. Simultaneously, an NTC resistor is implemented to sense whether there is any hot-spot of power circuit. If the voltage exceeds the external OTP trip level VCS>V_CSOTP (typical 0.8V), an internal counter has been added to prevent incorrect OTP detection. However, if Td_CSOTP of subsequent OTP events are detected, the external OTP protection is tripped.



Typical Application

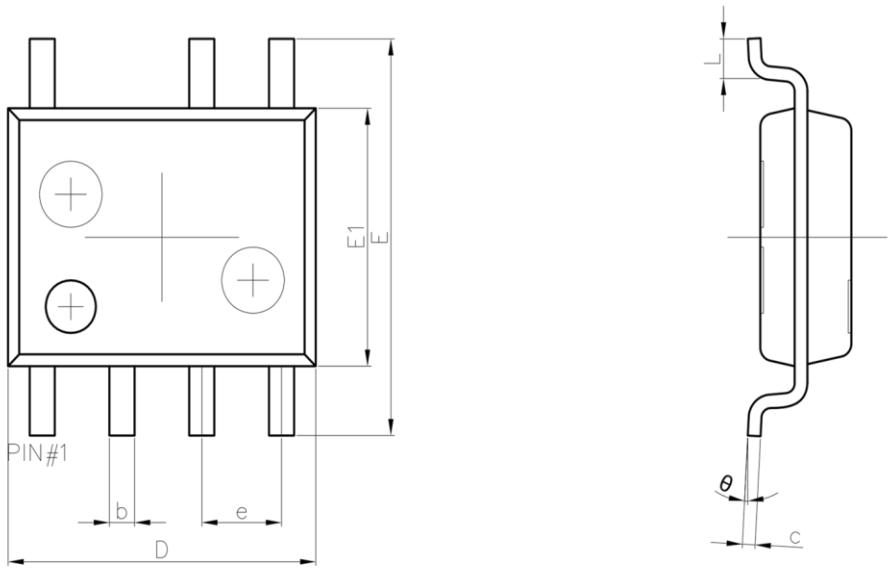


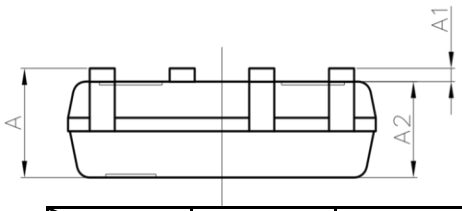
Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place from the VDD pin and the GND pin.

Package Information

Package Information SOP7





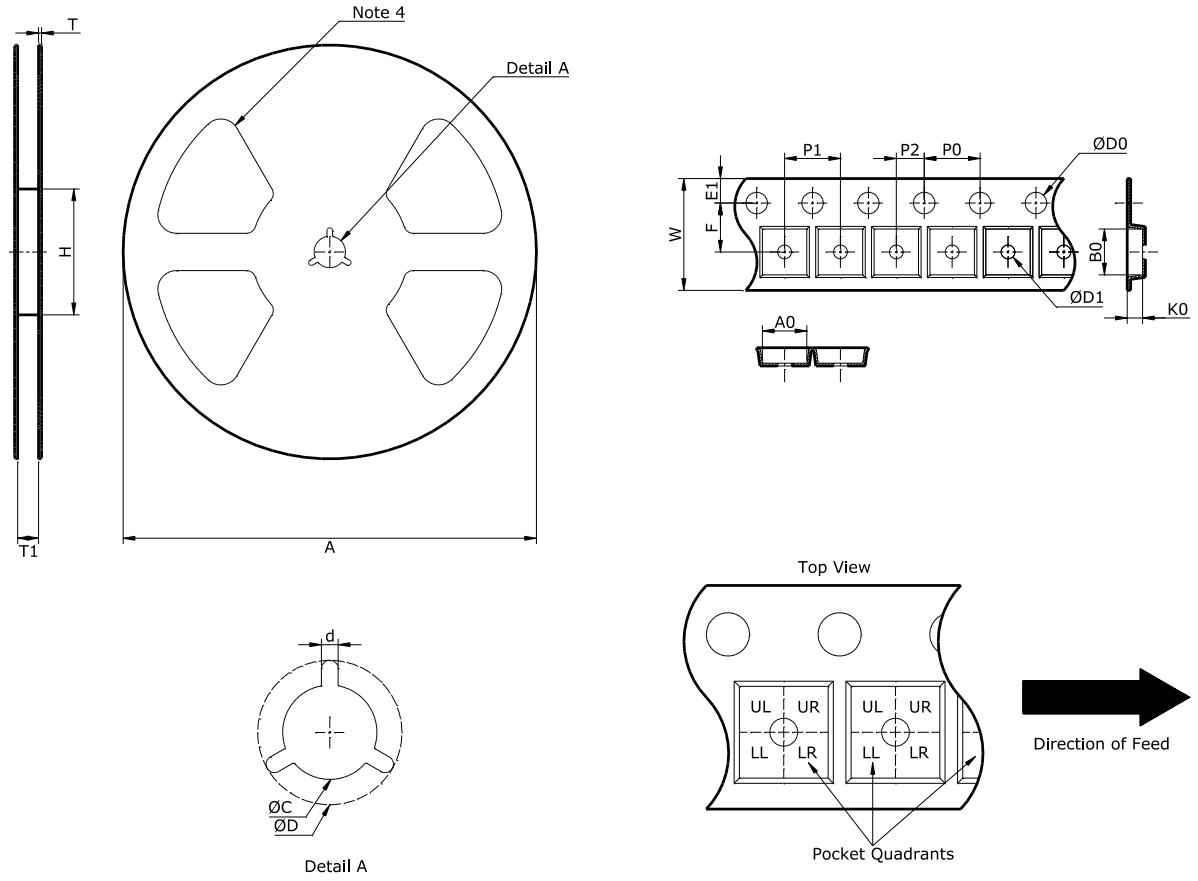
Size / symbol	Min.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Max.(mm)
A	1.350	1.750	E	5.80	6.20
A1	0.100	0.250	E1	3.80	4.000
A2	1.35	1.550	e	1.270(BSC)	
b	0.330	0.510	h	0.400	0.800
c	0.170	0.250	θ	0 °	8 °
D	4.700	5.100			

Top mark	Package
PN PN8273 YWWXXXXX	SOP7

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion

Tape and Reel Information



SOP7 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±1.0	2.6 +1/-0	12.4 +1/-0	100 ±0.5	12.00 +0.5/-0.2	17.70 ±0.40	1.9 ±0.40	6.40 ±0.1	5.4 ±0.1	2.1 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.3	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.05	1.5 +0.1/-0	1.55 +0.25/-0	UL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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